**Sonu Vishwakarma**

**PROFILE**

To aspire for a challenging position in a professional organization where I can enhance my skills and strengthen them in conjunction with the organization’s goal.

**EDUCATION**

* **M.Tech VLSI Design**

**CGPA – 7.34 / 10**

Amrita Vishwa Vidyapeetham

* **B.E Instrumentation Engineering**

**CGPA – 6.42 / 10**

University of Mumbai

* **Class 12** – 69.17%

Institution:

* **Class 10** – 70.92%

Institution:

**TECHNICAL INTERESTS**

VLSI Design

**PROJECTS**

**Router 1x3 Design using Verilog (PG)**   
The focus of the work is on designing a router that forwards the data packets between computer network depending upon the address present in the header of the packets.

Tools Used: ModelSim and Xilinx Vivado.

**Design and Detail Engineering of Tetra Hydro Fluorine Plant (UG)**   
This project aims to provide a practical insight into DESIGN and DOCUMENTATION. The documentation involves preparing a variety of documents and it gives an understanding of planning and estimation.

**TECHNICAL SKILLS**

ModelSim, Xlinx Vivado

**WORK EXPERIENCE**

**Metro Train Pilot,** Metro One Operation Pvt Ltd (Reliance Metro) for 2 years and 8 months of Experiences.

**Central Railway.**

Location and Duration : 15 days, Mumbai, Matunga.

Objective : In plant Training in Carriage Workshop.

**LANGUAGES**

English, Hindi, Marathi

**EXTRA CURRICULAR ACTIVITIES**

Knowledge of Digital Logic Design and Understanding of CMOS.

Hands on with Cadence Virtuoso tool for layout and Schematic and EDA tools like ModelSim, Vivado.

Knowledge of DETAIL & DESIGN ENGINEERING and Drawing Reading.